HIGH PERFORMANCE HEMT MMICs FOR LOW COST EHF SATCOM TERMINALS

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ABSTRACT

Presented is a set of high performance pseudomorphic InGaAs HEMT MMICs for insertion into a low cost transceiver for EHF SATCOM terminal applications. A 20 GHz MMIC LNA with 1.8 dB noise figure and 38 dB gain and a 44 GHz driver amplifier with an output power of +17.8 dBm, 22.8 dB gain, and 17% efficiency are featured. Also reported are HEMT MMIC doublers with output frequencies of 17, 22, and 44 GHz which demonstrate +13, +12, and +5 dBm power outputs with 1 dB conversion loss, 1 dB conversion gain, and 4 dB conversion loss, respectively.

INTRODUCTION

The performance and cost drivers of the transceiver for EHF SATCOM terminals include low noise figure, high reliability, small size and weight, and low power consumption [1]. For these reasons HEMT MMIC technology is a key to future systems. HEMT MMICs offer small size, high reliability, good producibility, easier assembly with no tuning, and performance that rivals or improves upon hybrid MICs. The 20 GHz LNA and 44 GHz driver amplifier presented here represent improved performance over previous results [2,3]. We believe the 20 GHz MMIC LNA to be the best reported to date with the 1.8 dB noise figure being 0.2 dB lower than previously reported and with 5 dB more gain. The MMIC doubler and 44 GHz driver amp performance is also the best reported to our knowledge. This work demonstrates that the critical components of the transceiver system can be fabricated using planar-doped pseudomorphic InGaAs HEMT technology.

TRANSCEIVER SYSTEM

Figure 1 shows a block diagram of the transceiver system. The receiver begins with the 20 GHz receive signal at the front end and the LNA is followed by a bandpass filter fabricated on 10 mil quartz. The LO chain utilizes a pair of MMIC distributed amplifiers fabricated using MESFET technology as gain blocks before and after the 17 GHz HEMT MMIC doubler. A MESFET downconverter chip is fed the 20 GHz RF signal and the 17 GHz LO signal and outputs the 3.29 GHz IF. A second downconversion brings the output IF signal to 70 MHz. The MESFET and commercial second IF parts were used on this project for low development cost. The LO signals are generated by a synthesizer and the IF is fed to the modem processor.

The 11 GHz synthesized signal for the transmit chain is amplified by a MESFET gain block and doubled by the 22 GHz HEMT MMIC doubler. After a 10 mil quartz bandpass filter the signal is again amplified and then doubled again by the 44 GHz HEMT MMIC doubler. After a final filter the signal is amplified by the 44 GHz driver amplifier and output to waveguide through a finline microstrip-to-waveguide transition.

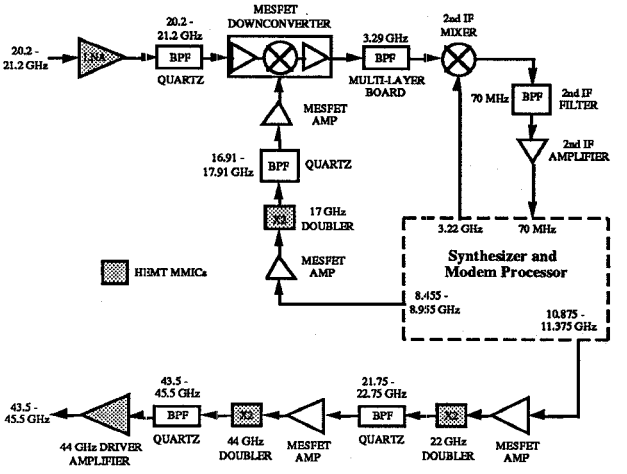

Figure 1. Transceiver System Block Diagram.

20 GHZ LOW NOISE AMPLIFIER

The 20 GHz LNA is shown in Figure 2. It is a three stage design featuring 120 μm devices fabricated with TRW's 0.2 μm low noise planar-doped pseudomorphic InGaAs T-gate HEMT process. Small-signal and noise models of the 120 μm HEMT were optimized to data measured from 2-26 GHz using the ATN noise parameter test-set. The noise figure and

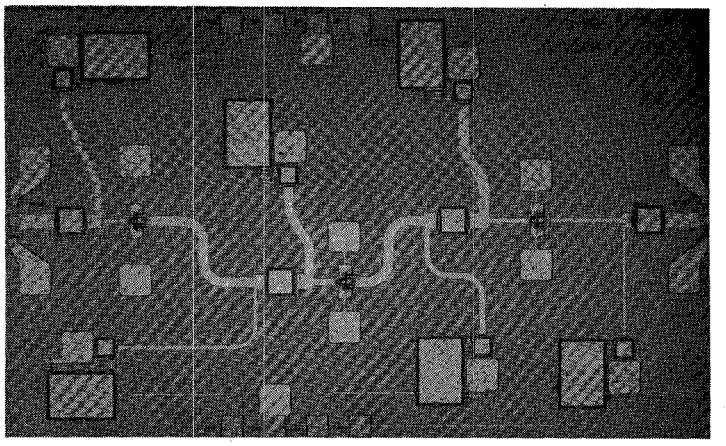

Figure 2. 20 GHz HEMT MMIC LNA, 3.4 mm x 2.1 mm.

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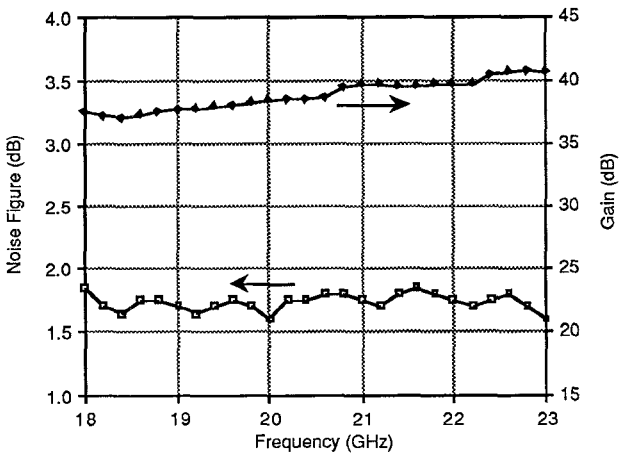

Figure 3. 20 GHz LNA with 1.8 dB NF and 38 dB Gain

associated gain of a typical amplifier circuit are shown in Figure 3. The noise figure of 1.8 dB and associated gain of greater than 38 dB are the best reported to date. This data was measured on-wafer with Cascade Microtech RF probes and an HP noise figure meter. A packaged LNA still shows less than 2 dB noise figure, including a finline waveguide-to-microstrip transition.

Three wafers processed for this project yielded 65%, 50%, and 43% RF good LNAs using a noise figure value of 2 dB as the benchmark. Good yield of such critical components as the LNA will help drive down the cost of the transceiver for future terminals.

HEMT MMIC DOUBLER DESIGN

The doublers are all single-ended and are designed around the general schematic shown in Figure 4. The input is matched at the fundamental frequency and gate bias is injected through a quarter-wavelength high impedance line and an on-chip bias network designed to keep the HEMT device stable under all conditions. Immediately following the drain of the device there is a quarter-wavelength open circuited stub to reflect the fundamental frequency back into the FET while allowing the doubler frequency to pass (since the line is a half-wavelength at the doubled frequency). This technique [4] improves the conversion loss of the circuit while also improving the fundamental rejection. The output network is then optimized to match at the doubled frequency and the drain bias is injected through a quarter-wave (at the doubled frequency) line.

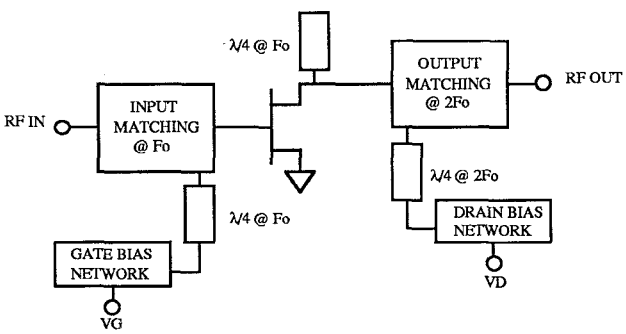

Figure 4. Schematic of HEMT MMIC Doublers.

The matching networks were designed to match 50 ohm input and output impedances to the HEMT device and the added effects of the bias networks and the quarter-wave rejection stub. An asymmetric Curtice FET model [5] was used to model the HEMT device under large signal conditions. The Curtice model was derived from measured S-parameter data to 40 GHz and DC I-V curves. The matching networks were then optimized to give the best output power and conversion loss over the frequency bands of interest.

17 GHZ HEMT MMIC DOUBLER

The key component in the receiver's local oscillator chain is the 17 GHz HEMT MMIC doubler. Figure 5 is a photo of the completed chip, which features a single 300 μm HEMT device. Figure 6 shows the measured Pout vs Pin performance and conversion loss of the doubler at 17.4 GHz. The doubler delivers +13 dBm output power with less than 1 dB conversion loss or +12 dBm with 0 dB conversion loss. Figure 7 shows the output power as a function of the output frequency from 16 to 19 GHz. The rejection of the fundamental input signal is better than 25 dB from 8 to 9.5 GHz.

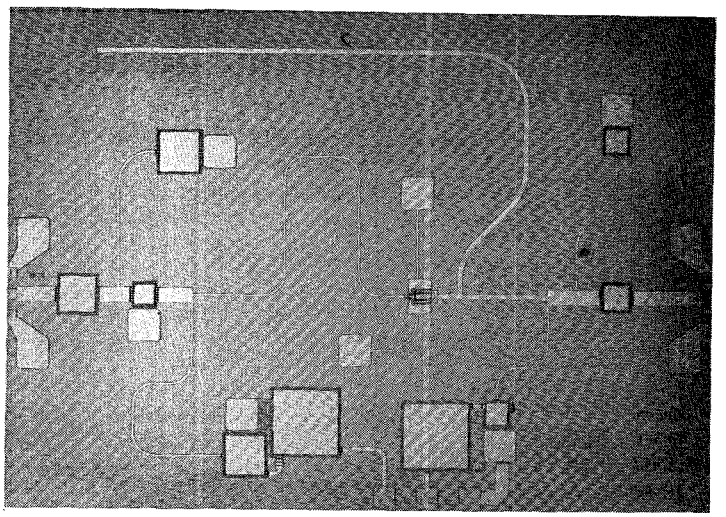

Figure 5. 17 GHz HEMT MMIC Doubler, 3.4 mm x 2.4 mm

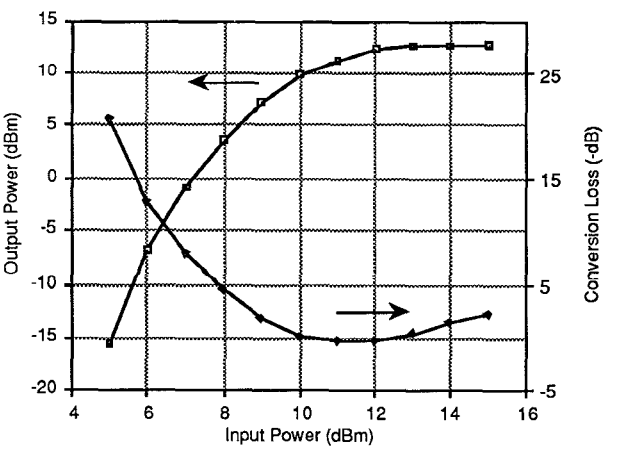

Figure 6. Pout and Conversion Loss of 17 GHz Doubler.

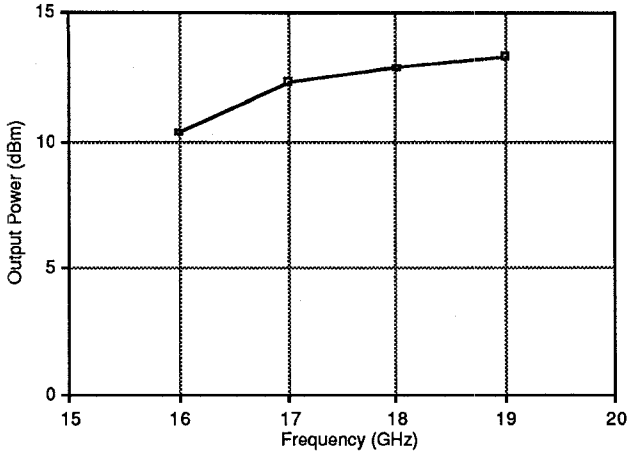

Figure 7. Pout vs. Freq. for 17 GHz Doubler, Pin = +13 dBm.

22 GHZ HEMT MMIC DOUBLER

The design of the 22 GHz HEMT MMIC doubler is similar to that of the 17 GHz doubler. The circuit again features a 300 µm HEMT device and the layout is very similar. Figure 8 shows the output power and conversion loss as a function of input power at an output frequency of 22.25 GHz. At +10 dBm input power the doubler delivers +11 dBm of output power, yielding 1 dB of conversion gain. Saturated output power is +13 dBm with a conversion loss of 1 dB. The output power as a function of frequency is shown in Figure 9 for an input power of +11 dBm and shows between +10 dBm and +11 dBm output power from 21 to 24 GHz.

44 GHZ HEMT MMIC DOUBLER

Figure 10 shows the completed 44 GHz HEMT MMIC doubler circuit. The design philosophy is identical to that used in the other doublers, but a 150 µm HEMT device is used for the 44 GHz design. The Pout vs Pin characteristics and conversion loss are shown in Figure 11 and the output power as function of frequency and for an input power of +8 dBm is shown in Figure 12. The circuit delivers about +5 dBm of output power from 42 to 47 GHz with 3 dB conversion loss.

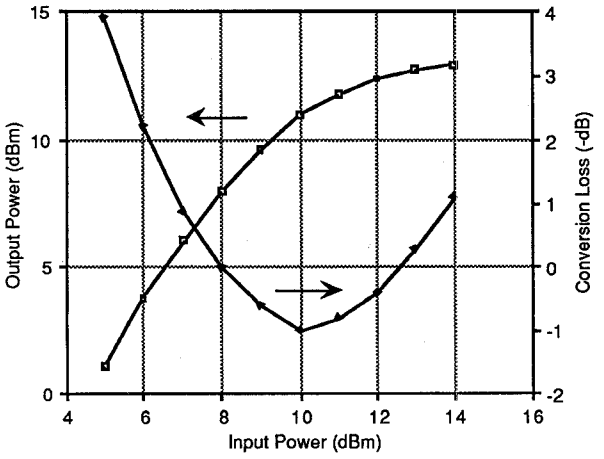

Figure 8. Pout and Conversion Loss of 22 GHz Doubler.

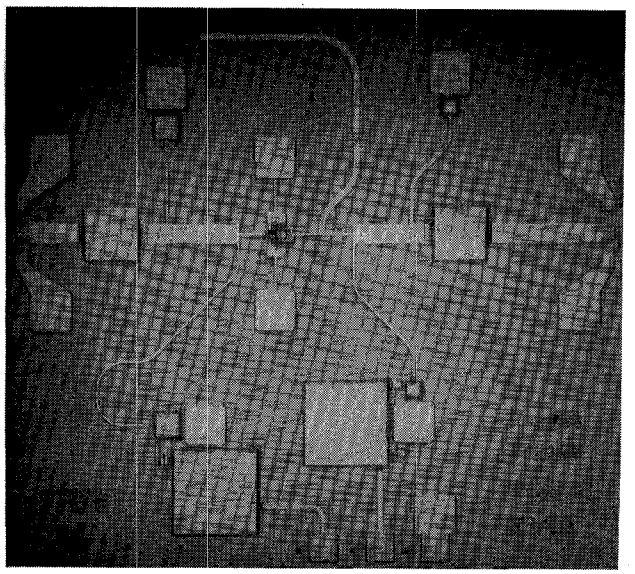

Figure 9. 44 GHz HEMT Doubler, 2.28 mm x 2.1 mm.

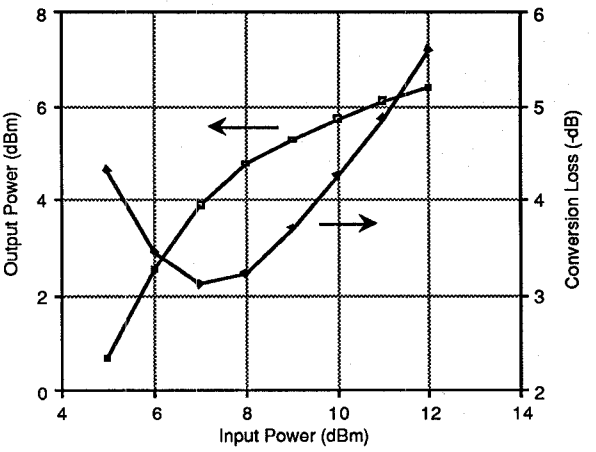

Figure 10. Pout and Conversion Loss of 44 GHz Doubler.

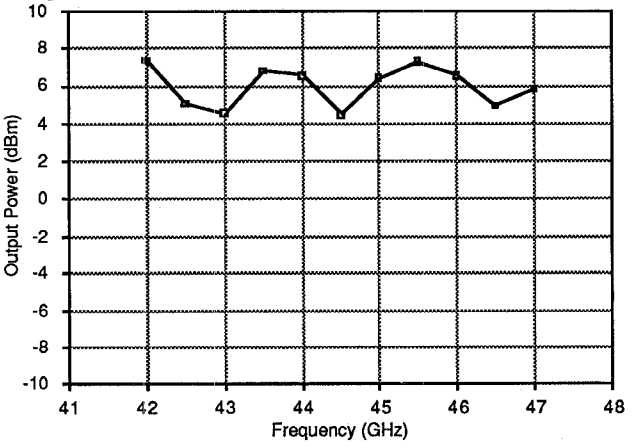

Figure 11. Pout vs. Freq. of 44 GHz Doubler, Pin = +8 dBm.

44 GHZ DRIVER AMPLIFIER

The completed 44 GHz driver amplifier is shown in Figure 12. It is a three stage design with 80 µm devices in the first two stages for good gain and a 150 µm device in the third stage for increased power performance. The circuit was designed using a model derived from device S-parameter measurements up to 40 GHz. The Curtice model 2 was also used in the design to help predict the circuit performance under large-signal conditions. Figure 13 shows the output power, gain, and efficiency for the amplifier as a function of input power at 44.5 GHz. The amplifier delivers 60 mW of output power with 23 dB gain and 17% efficiency. This data was measured at a drain bias of 4 volts. With a drain bias of 3 volts, the small signal gain is about 2 dB higher and the efficiency is better than 20%. The output power as a function of frequency is shown in Figure 14 for an input power of -5 dBm. The amplifier delivers flat output power of +16 dBm from 43 to 47 GHz.

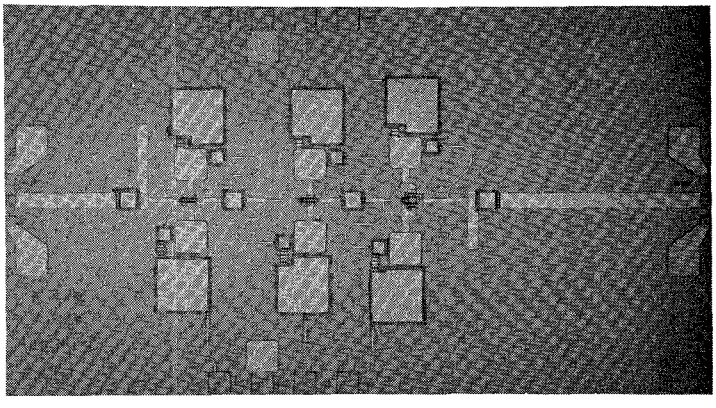

Figure 12. 44 GHz MMIC Driver Amp, 3.4 mm x 1.9 mm.

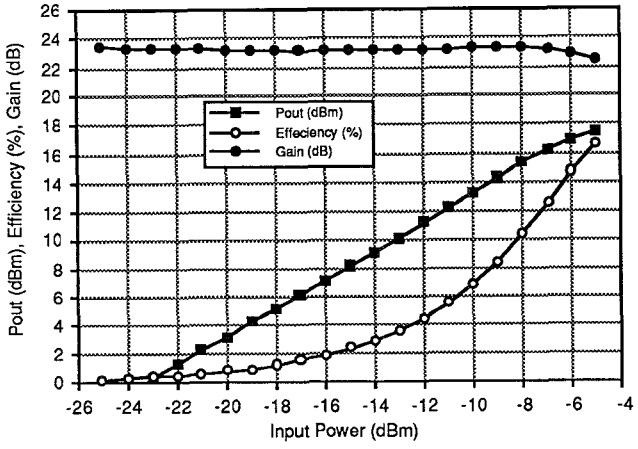

Figure 13. Pout, Gain, and Efficiency of 44 GHz Amplifier.

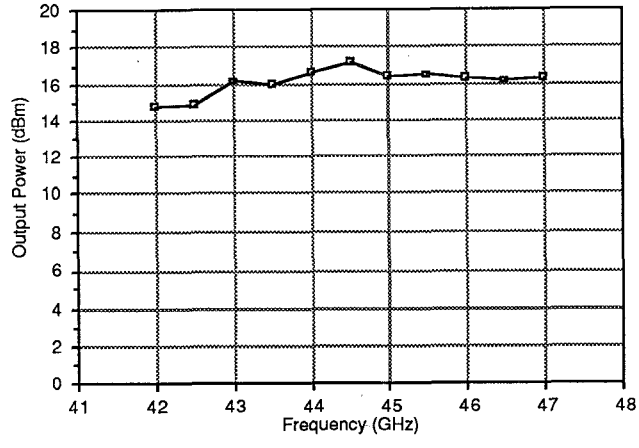

Figure 14. 44 GHz Amplifier Output Power vs. Frequency.

CONCLUSION

We have demonstrated superior performance in both low noise and power MMIC circuits utilizing the same InGaAs pseudomorphic HEMT process. The 20 GHz LNA with gain of 38 dB and a noise figure of 1.8 dB will be incorporated along with the 17 GHz HEMT MMIC doubler and the various MESFET MMICs, filters, and low-frequency parts in the receive portion of a transceiver system. The 22 and 44 GHz HEMT MMIC doublers will be incorporated with the 44 GHz HEMT MMIC driver amplifier, which delivers +17.8 dBm with 17% efficiency, to create a transmitter chain well suited for driving a 44 GHz power amplifier for terminal applications.

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